TX20N15A4L

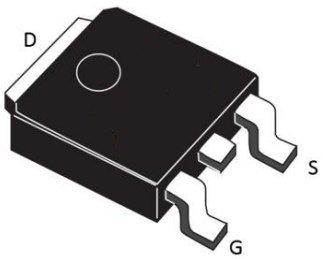
Silicon N-Channel Power MOSFET

General Description :

The TX20N15A4L uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is TO-252, which accords with the RoHS standard.

V_{DSS}	150	V
I_D	20	A
P_D	90	W
$R_{DS(ON)type}$	62	mΩ

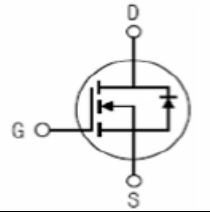
TO-252



Features :

- $R_{DS(ON)}$ <75mΩ @ V_{GS}=10V (Typ62mΩ)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Inner Equivalent Principium Chart



Applications :

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Absolute (Tc= 25℃ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	150	V
I_D	Continuous Drain Current	20	A
I_{DM}	Pulsed Drain Current	40	A
V_{GS}	Gate-to-Source Voltage	±20	V
P_D	Power Dissipation	90	W
E_{AS}	Single pulse avalanche energy[a5]	80	mJ
T_J , T_{stg}	Operating Junction and Storage Temperature Range	175 , −55 to 175	℃

Electrical Characteristics (Tc= 25℃ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	150	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=150V, V_{GS}= 0V,T_a=25℃	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+20V	--	--	0.1	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-20V	--	--	-0.1	μA

ON Characteristics[a3]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=10A	--	62	75	mΩ
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=4.5V,I_D=10A	--	65	80	mΩ
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=2.5V,I_D=10A	--	75	100	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	0.5	--	1.5	V
Pulse width tp≤380μs,δ≤2%						

Dynamic Characteristics[a4]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=5V,I_D=10A	--	20	--	S
C_{iss}	Input Capacitance	V_{GS}=0V,V_{DS}=75V f=1.0MHz	--	2500	--	pF
C_{oss}	Output Capacitance		--	150	--	
C_{rss}	Reverse Transfer Capacitance		--	54	--	

Resistive Switching Characteristics[a4]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=75V, R_L=5Ω V_{GS}=10V,R_G=3Ω	--	23	--	ns
tr	Rise Time		--	11	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	26	--	
t_f	Fall Time		--	11	--	
Q_g	Total Gate Charge	V_{DD}=75V, I_D=10A V_{GS}=10V	--	60	--	nC
Q_{gs}	Gate to Source Charge		--	7.5	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	17	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current [a2](Body Diode)		--	--	20	A
V_{SD}	Diode Forward Voltage[a3]	I_S=20A,V_{GS}=0V	--	--	1.2	V

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case[a2]	1.7	℃/W

[a1] : Repetitive Rating: Pulse width limited by maximum junction temperature.

[a2] : Surface Mounted on FR4 Board, t≤10sec.

[a3] : Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%.

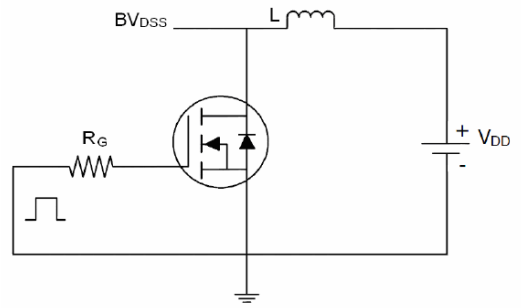
[a4] : Guaranteed by design, not subject to production

[a5] : EAS condition : Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

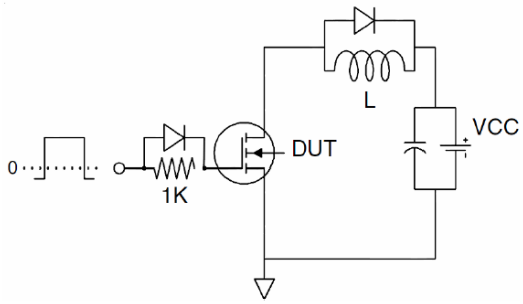
Test circurt

Silicon N-Channel Power MOSFET

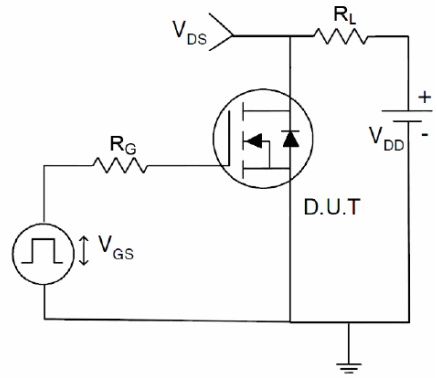
1) EAS test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Characteristics Curve :

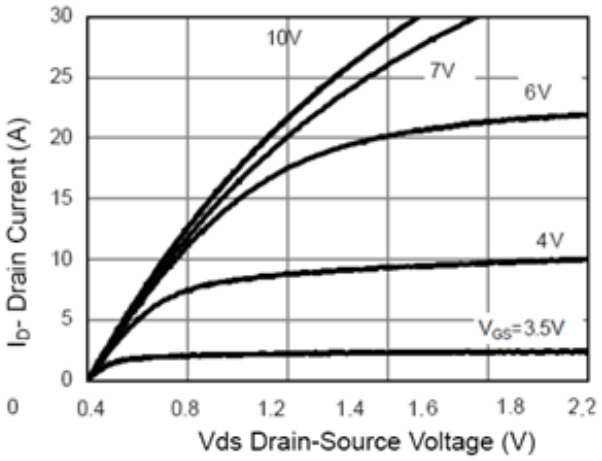


Figure 1 Output Characteristics

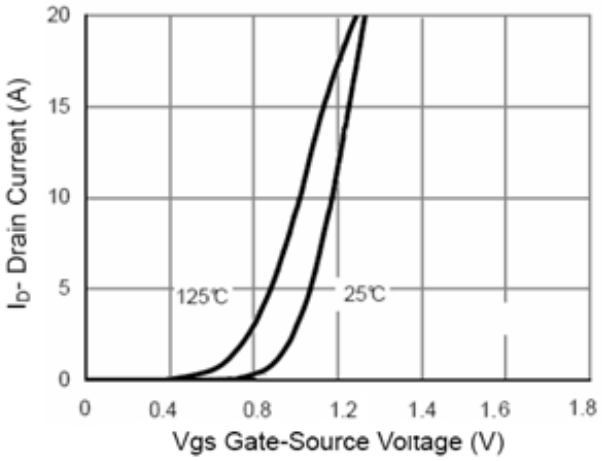


Figure 2 Transfer Characteristics

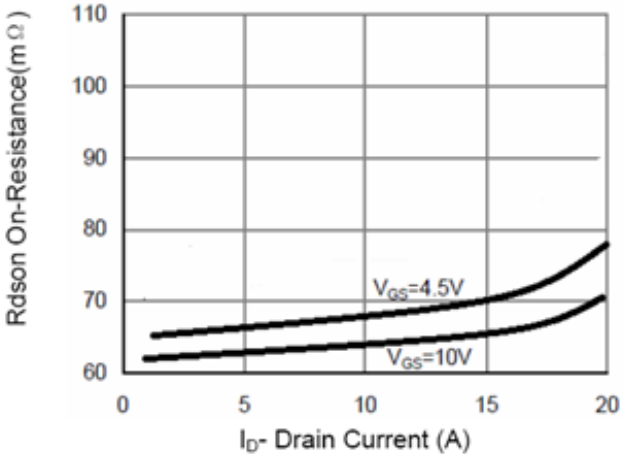


Figure 3 Rdson- Drain Current

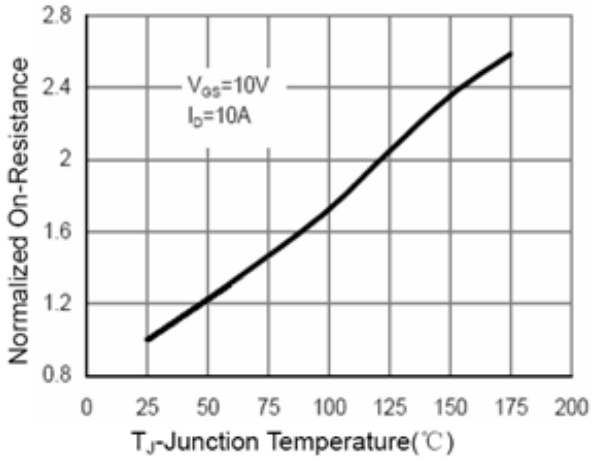


Figure 4 Rdson-JunctionTemperature

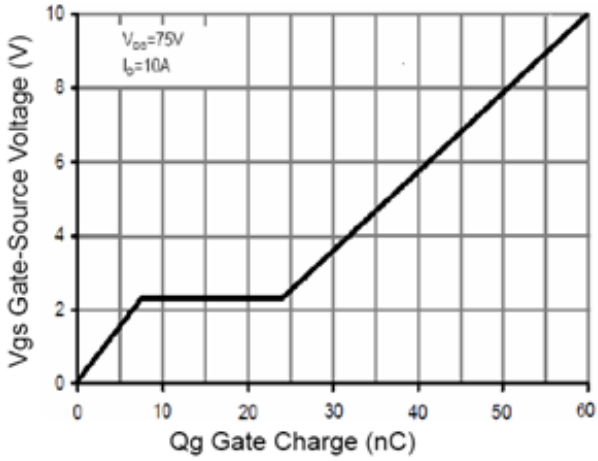


Figure 5 Gate Charge

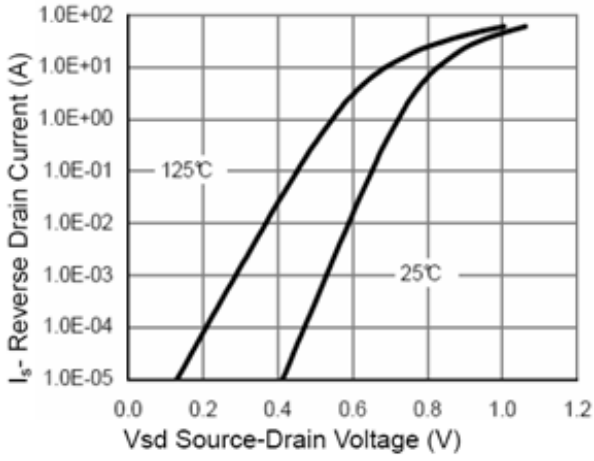


Figure 6 Source- Drain Diode Forward

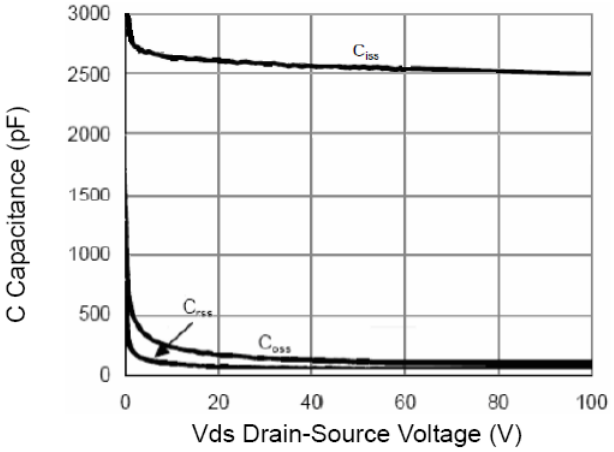


Figure 7 Capacitance vs Vds

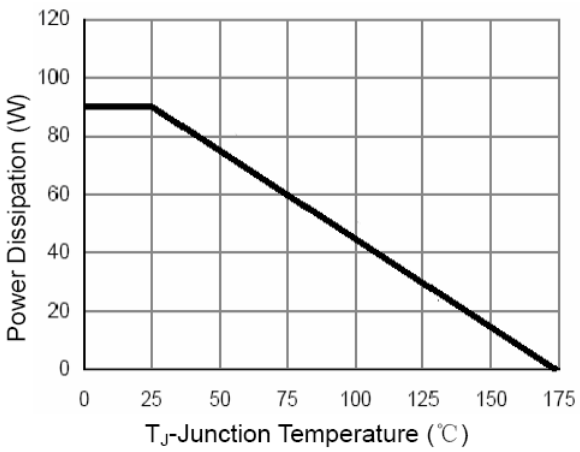


Figure 9 Power De-rating

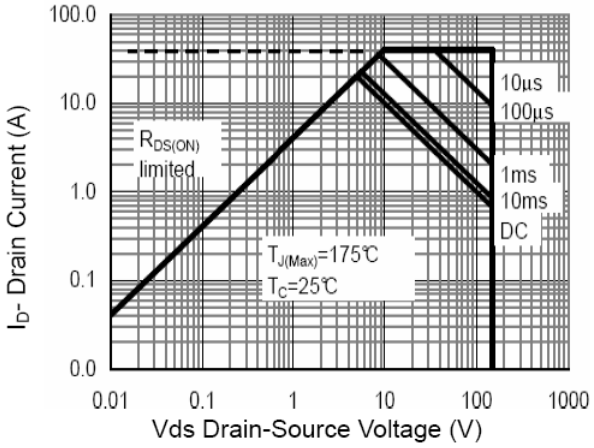


Figure 8 Safe Operation Area

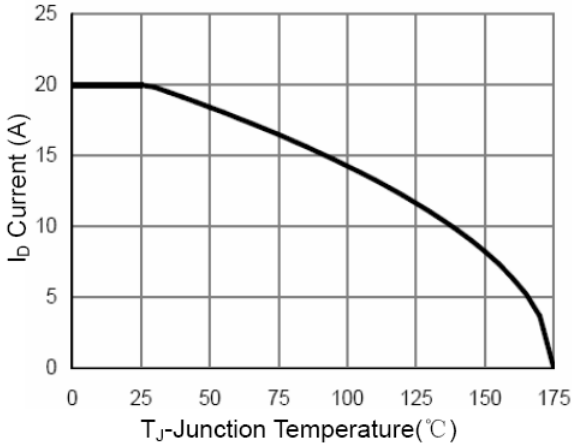


Figure 10ID Current- Junction Temperature

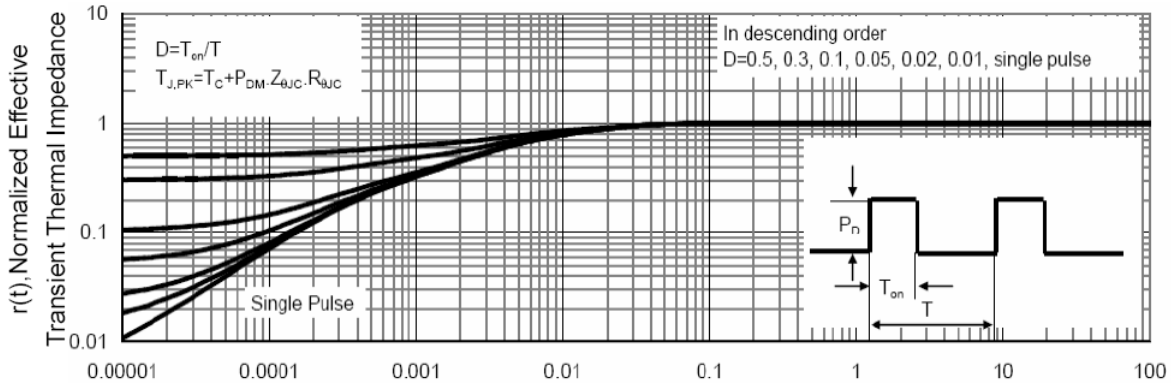
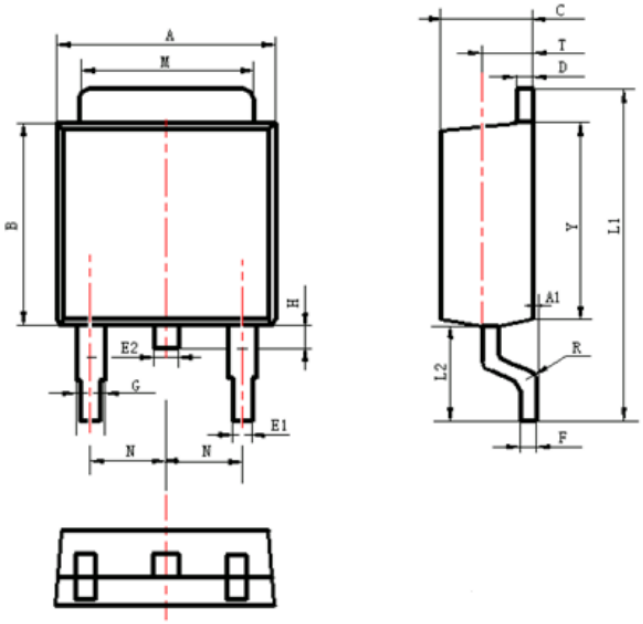


Figure 11 Normalized Maximum Transient Thermal Impedance

Silicon N-Channel Power MOSFET

Package Information：



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.16
B	5.70	6.30
C	2.10	2.50
D	0.30	0.70
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.40	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package